Hall Ticket Number:

Code No. : 12228 N/O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. II-Semester Main & Backlog Examinations, August-2023

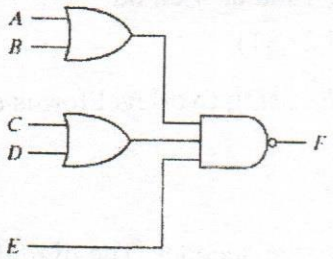
Logic and Switching Theory

(Common to CSE & AIML)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Convert the following numbers with the indicated bases to decimal: (a) $(4310)_5$ (b) $(435)_8$	2	1	1	1
2.	Convert the following expression to sum of products and product of sums: $x' + x(x + y')(y + z')$	2	1	1	1,2
3.	Find all the prime implicants for the following Boolean function, and determine which are essential: $F(A, B, C, D) = \sum (0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$	2	2	2	1
4.	Convert the following circuit to NOR-OR gate circuit. 	2	2	2	1,2
5.	Compare combinational circuit and Sequential circuit.	2	1	3	1
6.	A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram.	2	3	3	1,2,3
7.	Show that the characteristic equation for the complement output of a JK flip-flop is Q' (t + 1) = J'Q'+ KQ.	2	1	4	1,2
8.	Design a sequential circuit with two D flip-flops A and B, and one input x_in . When x_in = 0, the state of the circuit remains the same. When x_in = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats.	2	2	4	1,2,3
9.	The memory units that follow are specified by the number of words times the number of bits per word. How many address lines and input–output data lines are needed in each case? (a) 8K * 16 (b) 2G * 8	2	1	5	1,2
10.	List the types of ROMs and define each.	2	1	5	1

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Part-B (5×8 = 40 Marks)

11. a)	Consider a five-input Boolean function that is asserted whenever exactly two of its inputs are asserted : a) Construct the Truth Table for the function. b) Represent function in SOP form & POS form.	4	3	1	1,2,3
b)	The literal count of a Boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of (xy+xz) is 4. What are the minimum possible literal counts of the pos & sop representations respectively of the function given by the following Karnaugh map	4	3	1	1,2,3

xy \ zw	00	01	11	10
00	X	1	0	1
01	0	1	X	0
11	1	X	X	0
10	X	0	0	X

12. a)	Minimize the following expression by using Tabular Method $F(A,B,C,D,E) = \sum (0,1,2,8,9,15,17,21,24,25,27,31)$	4	2	2	1,2
b)	Implement the following Boolean function F, using two-level forms of logic (a) NAND-AND (b) NOR-OR $F(A, B, C, D) = \sum(10, 4, 8, 9, 10, 11, 12, 14)$	4	3	2	1,2
13. a)	Design a digital system using an appropriate size decoder. The digital system has output defined as logically high if the 4–bit input binary number is a multiple of 3; otherwise, the output will be logically low. The output is defined if andonly if the input binary number is greater than 5.	4	3	3	1,2,3
b)	An 8*1 multiplexer has inputs A, B, and C connected to the selection inputs S2, S1, and S0, respectively. The data inputs I0 through I7 are as follows: I1=I2=I7=0; I3=I5=1; I0=I4=D; and I6= D '. Determine the Boolean function that the multiplexer implements.	4	3	3	1,2
14. a)	For the following state table	4	2	4	1,2,3

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(a) Tabulate the reduced state table.

(b) Draw the state diagram corresponding to the reduced state table.

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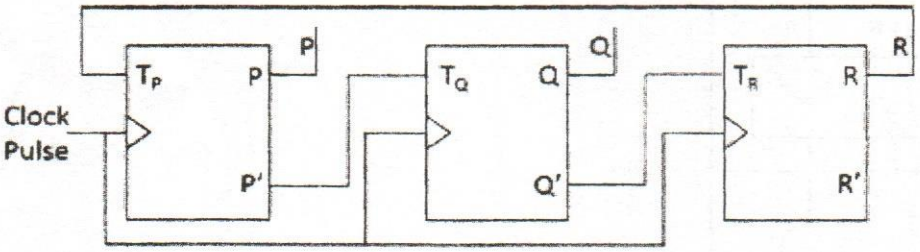
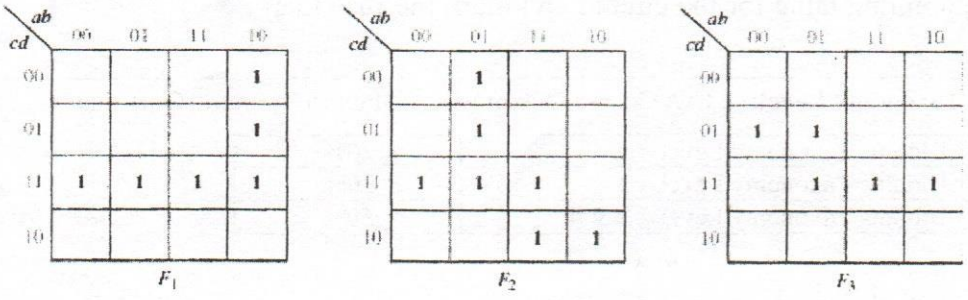
b)	Consider a 3 bit counter, designed using T flipflops. Assume initial state of counter given by PQR as 000. What are next three states:  	4	3	4	1,2
15. a)	Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number.	4	3	5	1,2,3
b)	Tabulate the PLA programming table and circuit for the two Boolean functions listed below. Minimize the numbers of product terms. A(x, y, z) = (1, 3, 5, 6) B(x, y, z) = (0, 1, 6, 7)	4	2	5	1,2
16. a)	Simplify the following Boolean function F , together with the don't-care conditions d , and then express the simplified function in sum-of-minterms form: $F(A,B,C,D,E)= \sum (0,1,3,5,,7,8,10,12,15,20,25)+d(4,9,31)$	4	3	1	1,2
b)	Find expressions which correspond to a two-level, minimum multiple output AND-OR realization of $F1, F2$, and $F3$ and convert into NAND network  	4	3	2	1,2,
17.	Answer any ***two*** of the following:				
a)	Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.	4	3	3	1,2,3

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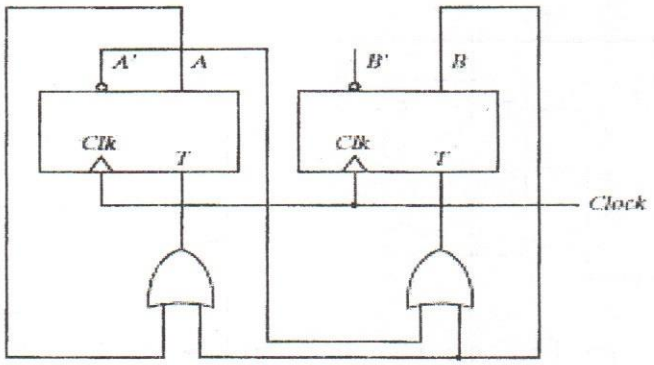
b)	Derive the state table and the state diagram of the given sequential circuit  	4	3	4	1,2,3
c)	The following is a truth table of three-input, four output combinational circuit: Input / Output x y z | A B C D 0 0 0 | 0 0 1 0 0 0 1 | 1 1 0 1 0 1 0 | 1 1 1 0 0 1 1 | 0 0 1 1 1 0 0 | 1 1 1 1 1 0 1 | 1 1 1 1 1 1 0 | 1 1 0 0 1 1 1 | 0 1 1 1 Tabulate the PAL programming table for the circuit, and mark the fuse map in a PAL diagram.	4	3	5	1,2,3

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	30%
iii)	Blooms Taxonomy Level – 3 & 4	50%

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